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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 1

Complete if Known	
Application Number	10/747,625
Filing Date	December 30, 2003
First Named Inventor	John P. DEVALE
Group Art Unit	Not yet assigned
Examiner Name	Not yet assigned
Attorney Docket Number	42339-193266

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1	Balasubramonian, R., et al. "Reducing the Complexity of the Register File in Dynamic Superscalar Processors." *Proc. of the 34th Int. Symposium on Microarchitecture (MICRO34)*, Dec. 2001.	
	2	Brekelbaum, N., et al., "Hierarchical Scheduling Windows." *Proc. of the 35th Int. Symposium on Microarchitecture (MICRO35)*, Nov. 2002.	
	3	Cruz, K. et al., "Multiple-banked Register File Architectures." *Proc. Of the Int. Symposium on Computer Architecture*, Jun. 2000.	
	4	Gonzalez, A., et al., "Virtual-physical registers." Proc. *of the 4th Int. Symposium on High Performance Computer Architecture*, Feb. 1998.	
	5	Hinton, G., et al., "The Microarchitecture of the Pentium 4® Processor." *Intel Technical Journal*, Q1 2001, pp. 1-13.	
	6	"Intel® Itanium® Architecture Software Developer's Manual." Intel Corporation 2002.	
	7	Jiménez, D. and C. Lin, "Dynamic Branch Prediction with Perceptrons," *Proc. of the 7th Int. Symposium on High Performance Computer Architecture (HPCA)*, 2001.	
	8	Kim, I. and Lipasti, M., "Half-Price Architecture." *Proc. of the Intl. Symposium on Computer Architecture*, 2003.	
	9	Kim, N., and Mudge, T., "Reducing Register Ports Using Delayed Write-Back Queues and Operand Pre-Fetch." *International Conference on Supercomputing*, 2003.	
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	16	Yung, R. and Wilhelm, N., "Caching Processor General Registers." *In Proceedings of the International Conference on Circuits Design*, 1995, pp. 307-312.	
	17	Borch, E., Manne, S., Emer, J., Tune, E., "Loose Loops Sink Chips." *The Proceedings of the 8th Int. Symp. on High Performance Computer Architecture*, 2002, pp. 1-12.	

Examiner Signature	Jacob Petrusek	Date Considered	3-20-06

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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